Introduction

The DS2762 High-Precision Battery Monitor provides monitoring and protection for a Li+ cell. When the device powers up, the state of the DQ pin, the Power Mode bit (PMOD) and the battery voltage can affect what mode the device enters and how the Charge Control (CC) and Discharge Control (DC) pins react. This Application Note will provide details of what happens in many possible powering up scenarios.

Powering Up a DS2762

When a DS2762 goes through its power on reset (POR) sequence, it begins in Active Mode and then makes a decision based on the cell voltage, the state of the DQ pin, and the PMOD bit to determine if it needs to go into Sleep Mode. The SWEN bit does not effect the actions of the DS2762 when it powers on.

In the following powering up cases of the DS2762, all device EEPROM is recalled to the shadow RAM during the POR sequence. Also, the state of the Accumulated Current Register (ACR) and the User RAM are undefined at power up.

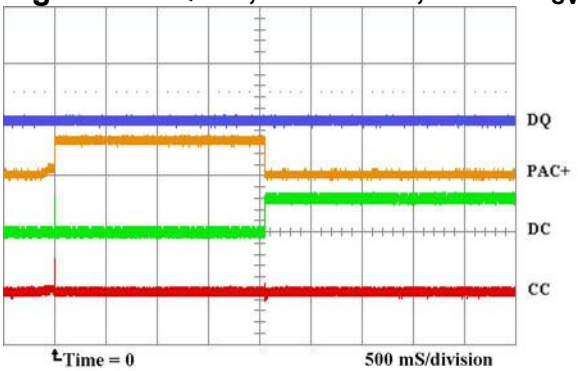
The following table contains the conditions at power up that will be examined in this Application Note.

CASE	POWER UP CONDITIONS			
	PMOD	SWEN	DQ	V_{IN}
A	1	--	0	> V_{UV}
B	--	--	0	< V_{UV}
C	0	--	0	> V_{UV}
D	--	--	1	> V_{UV}
E	--	--	1	< V_{UV}

Case A: DQ = 0, PMOD = 1, Cell > V_{UV}

If DQ is low and PMOD is 1, the DS2762 powers up in Active Mode with the CC and DC pins driven low to enable the PAC+ output. The device then enters Sleep Mode when it has detected that DQ has been low for 2 seconds. At that time, the DC pin is pulled to the cell voltage, which disables the PAC+ terminal. The PAC+ terminal is pulled low when the device is in Sleep Mode. The CC pin is pulled to PAC+, so that CC is low, but the charge FET is now disabled.

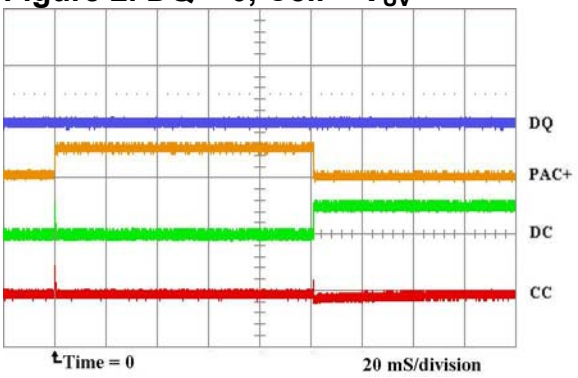
Figure 1. DQ = 0, PMOD = 1, Cell > V_{UV}



Case B: DQ = 0, Cell < V_{UV}

If all conditions are the same as Case A, except the cell voltage is below V_{UV}, the device enters Sleep Mode 100ms after powering up when the under voltage condition is detected. When the device enters Sleep Mode, the DC pin is pulled to the cell voltage, which disables PAC+, and the CC pin is pulled to PAC+, so that CC is low, but the charge FET is now disabled. In this case, PMOD has no effect on the behavior of the DS2762.

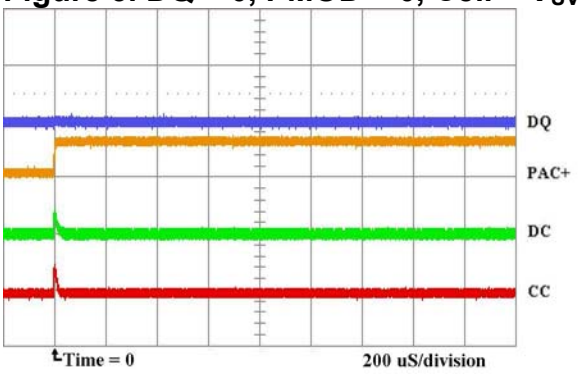
Figure 2. DQ = 0, Cell < V_{UV}



Case C: DQ = 0, PMOD = 0, Cell > V_{UV}

If DQ is low and PMOD is 0 when the DS2762 powers up above V_{UV}, the device immediately enters Active Mode and stays there. The CC and DC pins are driven low at power up and do not change.

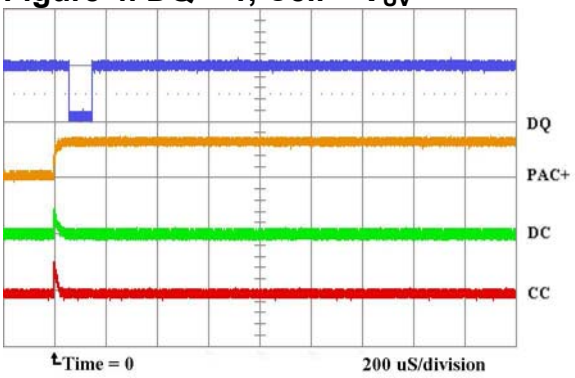
Figure 3. DQ = 0, PMOD = 0, Cell > V_{UV}



Case D: DQ = 1, Cell > V_{UV}

If DQ is high when the DS2762 powers up above V_{UV}, the device immediately enters Active Mode and stays there. DQ is pulled low by the DS2762 as it responds to a presence detect when powering up. The CC and DC pins are driven low at power up and do not change after that. PMOD has no effect on the behavior of the DS2762 in this case.

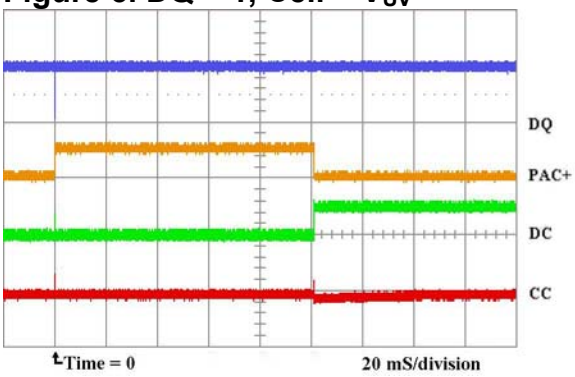
Figure 4. DQ = 1, Cell > V_{UV}



Case E: DQ = 1, Cell < V_{UV}

If all conditions are the same as Case D, except the cell voltage is below V_{UV}, the waveforms are identical for the first 100ms. However, after 100ms, the under voltage condition is detected and the device goes into Sleep Mode. At which time the DC pin is pulled to the cell voltage, which disables PAC+. The CC pin is driven low for the first 100ms and then as the device enters Sleep Mode, the CC pin is pulled to PAC+ so that it remains low, but the charge FET is now disabled.

Figure 5. DQ = 1, Cell < V_{UV}



Summary

The state of the protection pins at the time that power is applied to the DS2762 depends on the settings of the PMOD bit, the DQ line and the cell voltage. This is important when designing circuits and software to recover from an event that causes the device to temporarily lose power.